# Growth and characterization of GaAs epitaxial layers on Si/porous Si/Si substrate by chemical beam epitaxy

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The initial growth of GaAs films on a Si/porous Si/Si (SPS) substrate has been investigated using reflection high-energy electron diffraction. The morphology and the thickness have been examined by a Nomarski optical microscope and scanning electron microscope, respectively. The results of the low temperature photoluminescence studies have shown that a significant reduction in the residual thermal tensile stress can be achieved with reduced growth temperature. The 77 K photoluminescence spectra for GaAs/Si show a strain-induced splitting between the heavy and light hole valence bands which corresponds to a biaxial tensile stress of 2.45 kbar acting on the GaAs layer where the same for GaAs/SPS grown at 450 °C is 1.69 kbar. The results have shown that a SPS substrate with the combination of low temperature growth is a promising candidate for obtaining GaAs films with low stress. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1362339]

## INTRODUCTION

There has been considerable interest and extensive work over the past several years in the epitaxial growth of GaAs films on Si substrates for optoelectronics applications.[1] Recently, several techniques[2,3] have been proposed to obtain GaAs films on Si with good surface morphology. Recent research has shown that the problem caused by a large lattice mismatch between GaAs and Si, could be solved by using a low temperature grown GaAs buffer layer. Thermal stress can hardly be avoided in heteroepitaxial structures. However, from the extensive investigations of strained epitaxial layers, the reduction of thermal stress has been demonstrated clearly by selective-area growth and a postgrowth patterning technique.[4] The stress reduction is also achieved by doping a small amount of indium in the GaAs epitaxial layers on Si substrates.[5]

Porous silicon (PS) has been widely investigated in the last few years as a challenging new material for microelectronic devices.[6] The observation of photoluminescence[7] in PS has launched an intense research activity because this discovery has opened the door for a possible optoelectronic role for silicon, the all-important material for microelectronics.[8] Extensive studies have also been devoted to the application of PS in the electric isolation of integrated devices, in particular, the fabrication of a silicon on insulator substrate.[9] Recently, we[10] have demonstrated the reduction of stress in the GaAs layer on the Si/porous Si/Si (SPS) substrate by metalorganic chemical vapor deposition (MOCVD). In contrast to the selective-area growth or post-growth patterning techniques, the growth of GaAs/SPS is applicable for large area.

GaAs films have been grown on SPS substrates by chemical beam epitaxy (CBE) in anticipation that the thermal stress would be reduced by the low growth temperature as compared to MOCVD. Because of the presence of the small pores, porous Si layers are considered to be a flexible material. We, therefore, expect that the stress due to the large lattice mismatch and thermal expansion coefficient, is relaxed by straining small crystalline columns in porous Si layers, instead of the formation of misfit dislocations in GaAs films, and then GaAs films with good crystalline quality are grown on the SPS substrates.

In this article, we report on the study of the initial stages of GaAs growth on a SPS substrate with the use of reflection high-energy electron diffraction (RHEED). The quality of the GaAs on a SPS substrate grown at various temperatures have been determined by scanning electron microscope (SEM) and low temperature photoluminescence (PL).

## EXPERIMENT

A 12.6-$\mu$m-thick porous Si was formed by anodizing a heavily boron-doped (0.01–0.02 $\Omega$ cm) Si (100) wafer in 49% HF:$C_2H_5OH$ (2:1) solution. The etch current density was 7 mA $cm^{-2}$. A high-resolution SEM observation has

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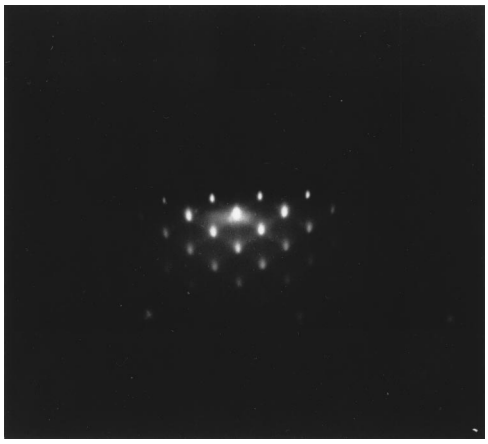

FIG. 1. RHEED pattern obtained from an as-deposited 20 nm GaAs nucleation layer on a Si/porous Si/Si substrate along a ⟨110⟩ azimuth.

shown that the size of surface pores is 6–8 nm in diameter, and the pore density is $\sim 1\times 10^{11}$ cm$^{-2}$.[11] The surface and inner pore walls were slightly oxidized at 400 °C in dry $O_2$ ambient, in order to cover the inner pore walls with a thin oxide film that prevented the coarsening of inner pores during the following heat treatments. This thin oxide at the porous surface was removed by HF dipping prior to the epitaxy. Around 10 nm single crystalline Si was epitaxially grown on the porous Si at 1060 °C by chemical vapor deposition in conjunction with hydrogen prebaking.[12]

The SPS substrates were degreased in organic solvents and etched by $H_2SO_4:H_2O=4:1$ solution. Finally, the substrate was hydroterminated using HF solution. The source gas for group III was triethylgallium and that for group V was arsine. Two step growth was employed for the heteroepitaxial growth of GaAs on the Si substrates. After the growth of 20 nm initial layer at 300 °C a 1 $\mu$m undoped GaAs layer was grown at different temperatures (450, 500, and 550 °C).

Low temperature photoluminescence measurements were made with the samples mounted in strain-free manner on a cold finger. Excitation was provided by an $Ar^+$ laser (514.5 nm). The luminescence from the sample was analyzed by a scanning spectrometer and detected by a photomultiplier. The spectra were recorded after lock-in amplification.

## RESULTS AND DISCUSSION

Figure 1 depicts the RHEED pattern obtained by diffracting along a ⟨110⟩ type azimuth of the 20 nm GaAs film on a SPS substrate immediately after low-temperature growth. From the figure it is clear that the layer is epitaxial with respect to the Si substrate as is evidenced by the presence of the distinct spots. We studied the surface morphology of the CBE-grown GaAs/SPS at various growth temperature of the top layers. The surface morphology depended on the growth temperatures of the top layer. The surface morphology of 450 °C grown GaAs epilayer on a SPS substrate under the Nomarski condition is shown in Fig. 2(a). From the figure, it is clear that when compared to GaAs/Si, the morphology is slightly rough. The roughness increases gradually as the growth temperature is increased. In order to

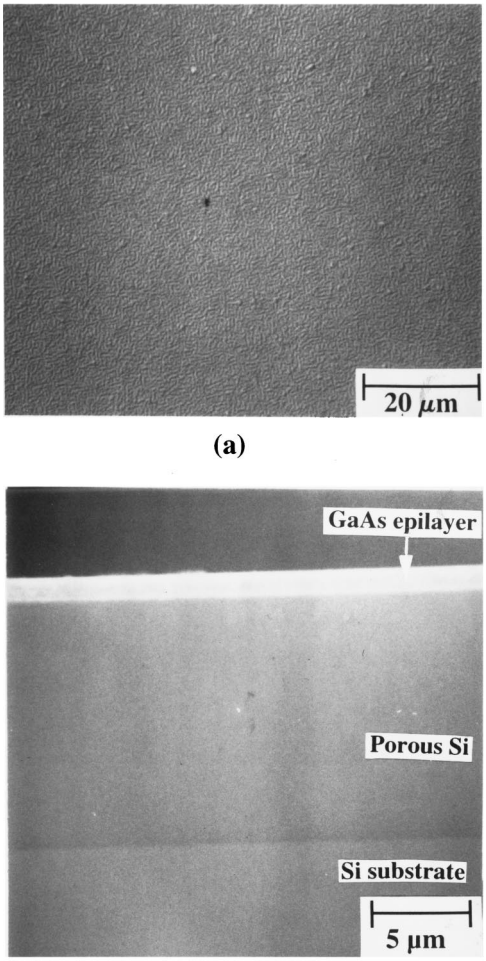


FIG. 2. Surface morphology (a) and cross-sectional SEM image (b) of a GaAs epitaxial layer on a Si/porous Si/Si substrate.

find the cause for the increased roughness of the epilayer we examined the morphology of the 20 nm nucleation layer. Though too small to be detected using standard optical, or Nomarski phase-contrast microscopy, the roughness of the 20 nm nucleation film does appear to slightly increase in the case of 20 nm GaAs on SPS substrate when compared to GaAs/Si. Using a model NT 2000-three dimensional *ex situ* noncontact optical interferometer from WYKO Inc., the surface roughness measured from GaAs/Si was 51.2 Å rms and GaAs on SPS was found to be slightly larger at 75.5 Å rms for 300 °C grown 20 nm GaAs layers. Figure 2(b) shows the cross-sectional scanning electron microscope image of a 1 $\mu$m GaAs epitaxial layer on a SPS substrate. From Fig. 2(b) it is clear that the grown GaAs epilayer is uniform and the interface between 12.6 $\mu$m porous Si and Si substrate is clearly visible.

The photoluminescence spectrum was measured to characterize the optical quality of the 1-$\mu$m-thick GaAs films. Figure 3 shows the 77 K photoluminescence spectrum of the GaAs on GaAs grown at 500 °C, GaAs on Si grown at 500 °C, and GaAs on SPS for three different growth temperatures (450, 500, and 550 °C). The 77 K PL intensity of the homoepitaxial GaAs is around 4.5 times higher than that

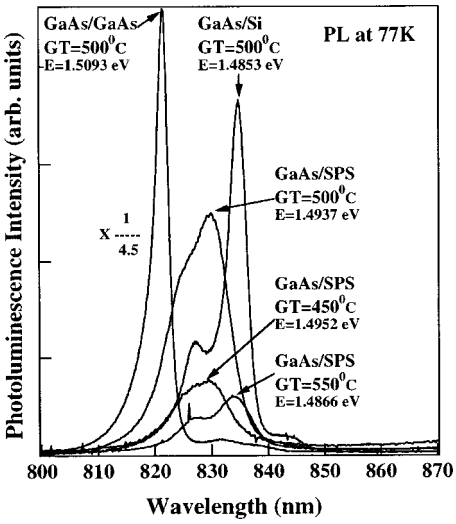


FIG. 3. 77 K photoluminescence of a CBE-grown GaAs epilayer on GaAs, Si, and Si/porous Si/Si substrates.

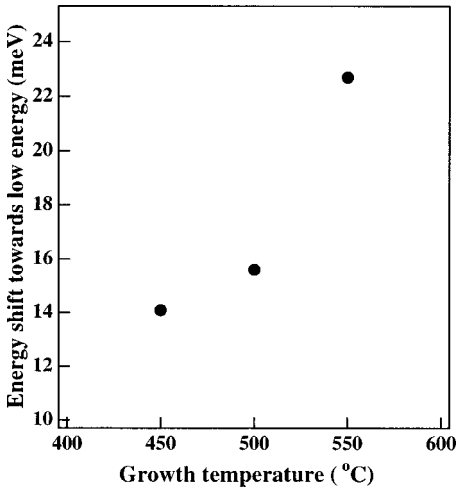


FIG. 4. Energy shift towards the low energy region in the growth of GaAs on a Si/porous Si/Si substrate when compared to CBE-grown GaAs/GaAs at 500 °C.

of heteroepitaxial (GaAs/Si) epilayer. The intensity of 500 °C grown GaAs epilayer on a SPS substrate is slightly less when compared to GaAs/Si. The *ex situ* noncontact optical interferometer observation shows that RMS roughness values of 500 and 550 °C grown GaAs epilayer on a SPS substrate are 9.56 and 17.32 nm where the same for GaAs/Si is 6.36 nm. The decrease in intensity in the case of 500 °C grown GaAs epilayers on SPS can be attributed to the increased roughness of the GaAs epilayer, due to the presence of porous region in the SPS substrate. In the case of 550 °C grown GaAs after the growth, we observed many small holes near the edges of the SPS substrate. Though the origin of these holes is not clear at this stage, this may lead to poor morphology and high roughness. The high roughness substantially reduce the intensity of GaAs grown on a SPS substrate at 550 °C. In all the growth, the prebaking has been carried out for 5 min at 50 °C above the growth temperature of the top layer. Hence, for the epilayer grown at 450 °C, the prebacking has been carried out at 500 °C. This temperature may not be sufficient enough to remove the oxidized layers on the SPS substrate. This could be the reason for the high roughness (rms roughness=14.15 nm) and reduction in PL intensity in the case of 450 °C grown epilayer.

We have observed two distinct emissions at 827.1 nm (1.4989 eV) and 834.7 nm (1.4853 eV) in GaAs on a Si substrate grown at 500 °C. In contrast, the GaAs/GaAs grown at 500 °C has the band edge emission peak at 821.4 nm (1.5093 eV), which is 24 meV higher than the peak at 834.7 nm in the GaAs/Si. As the biaxial strain causes a shift and split in the valence band of the GaAs layer, the peaks at 827.1 nm ($D^0$, lh) and 834.7 nm ($D^0$, hh) in the GaAs/Si are presumably due to the recombination involving excitons bound to Si donors and the $m_j = \pm 1/2$ (light hole) and the $m_j = \pm 3/2$ (heavy hole) valance-band states, respectively.[13] This demonstrates that the band edge emission peak of GaAs/Si is shifted and splits into two peaks due to the biaxial stress.

It can be observed that the heavy hole peak shift of GaAs/SPS is smaller than that of GaAs/Si. As shown in Fig. 4, the peak position of GaAs/SPS grown at 450 and 500 °C has shifted towards low energy by nearly 14.1 and 15.6 meV, respectively, as compared to GaAs/GaAs, whereas the same for GaAs/Si is 24 meV. This indicates that the stress in the epilayer has greatly reduced. In the case of 550 °C grown GaAs on SPS, the peak position is shifted towards low energy around 22.7 meV. The reason for this shift in the peak position may be due to the thermal strain introduced during cooling is easily absorbed by the porous region by straining small crystalline columns in a porous Si layer. In the case of 550 °C grown GaAs the peak position is almost the same as that of GaAs/Si since the large thermal stress could not be absorbed in the present porous layer.

The difference in the energy between the electron to light hole, and the electron to heavy hole transitions provides a measure of in-plane stress. Furthermore, this stress is tensile in nature, and arises from the difference in thermal expansion coefficients between GaAs and Si. For the biaxial stress parallel to [100] and [010], the calculated energy differences between the conduction and valence bands, and $k = 0$, were given as[14]

$$\Delta E_{1h} = -2a(S_{11}+2S_{12})X + b(S_{11}-S_{12})X, \quad (1)$$

$$\Delta E_{hh} = -2a(S_{11}+2S_{12})X - b(S_{11}-S_{12})X. \quad (2)$$

Here, $S_{11}$, $S_{12}$ are elastic compliances and $a$, $b$ are deformation potentials corresponding to hydrostatic and tetragonal shear deformation potentials, respectively, and $X$ is the stress acting on the layer. Both equations neglect higher-than first order terms in stress. From Eqs. (1) and (2), the valence-band splitting is equal to $2b(S_{11}-S_{12})X$. Using the values of $S_{11}$, $S_{12}$, $a$, and $b$ from the early report,[15] together with the experimentally determined valence-band splitting at 77 K, the biaxial tensile stress $X$ has been calculated as 2.45 kbar for GaAs/Si grown at 500 °C. The peak position of ($D^0$, lh) and ($D^0$, hh) transitions for 450 and 500 °C grown GaAs on a SPS substrate is determined by using a Gaussian peak fit. From Fig. 5 it is clear that the biaxial tensile stress for GaAs/SPS grown at 450 and 500 °C has reduced drastically to 1.69

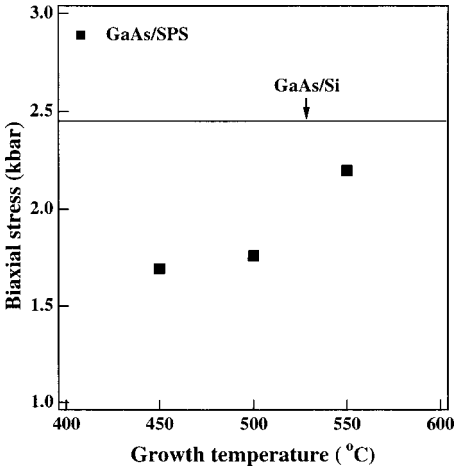


FIG. 5. Variation of biaxial tensile stress ($X$) due to GaAs epilayer growth temperature.

and 1.76 kbar, respectively, where the 550 °C grown GaAs/SPS is 2.19 kbar. Thus, we attribute the decrease in the biaxial tensile stress in the GaAs grown on SPS is caused by the presence of a porous region in the substrate and the low growth temperature.

## CONCLUSION

A GaAs epilayer has been grown on a SPS substrate for various temperatures. The surface morphology and the cross section of the grown epilayer have been examined by a Nomarski optical microscope and SEM, respectively. From the reduction of 77 K PL, the energy shift towards the low energy region proves that the stress has greatly reduced in the epitaxial layers grown on SPS substrates. PL measurements have been used to compare the thermally induced stress present in GaAs layers grown on both Si and SPS substrates. The energy splitting between the ($D^0$, lh) and ($D^0$, hh) transitions, at $T=77$ K, reflects a biaxial tensile stress of as low as 1.69 kbar for GaAs/SPS, grown at 450 °C. The earlier result shows that SPS and low temperature growth are promising candidates for obtaining GaAs films with low stress.

## ACKNOWLEDGMENT

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